









*technology introductions will introduce test requirement uncertainty and testing challenges to both the product developer and maintainer in the field.*

### *B. Multicore Processors/Parallel Programming*

Since the advent of the microprocessor, processor manufacturers improved the performance of Central Processing Units (CPUs) by architectural advances and by increasing clock speed by reducing the minimum feature pitch size on the die. Processor companies have begun implementing multiple “cores” within a processor, arranged in a parallel, closely coupled, architecture to increase effective processor throughput on multi-threaded tasks or tasks that can utilize Single Instruction, Multiple Data (SIMD) programming paradigms that enables algorithms to be spread across multiple cores. Manufacturers (Intel, IBM, and others) are packaging multiple CPUs on one chip in order to circumvent speed and power issues in classical processor development. When running on a multi-core system, multitasking Operating Systems (OS), such as Microsoft™ Windows™ can execute multiple tasks concurrently. The multiple computing engines work independently on different tasks (e.g., SI spectrum analysis on input port A and SI time domain analysis on input port B).

*It is envisioned that in future applications of SI multi-core computing, engines will work independently in controlling different tasks on independent multi-channel SI. Emerging trends such as parallel programming and associated facilitating tools which assist the user in visualizing and designing parallel code will be of extreme benefit in the application of multi-core processors in support of multichannel SI-based systems, where each channel runs a different application program in support of multiple UUTs or different I/O ports /pins on the same UUT concurrently.*

### *C. Low Phase Noise/Fast Switching Microwave Synthesizers*

Frequency synthesizers are fundamental to the operation and performance of SI (see Figure 1). Historically, two critical (and opposing) parameters have influenced synthesizer selection and performance: phase noise and frequency switching speeds. Traditionally, frequency synthesis has been performed by a number of mainstream direct and indirect techniques such as: Direct Analog Frequency Synthesis (DAFS), Direct Digital Synthesis (DDS), and Indirect or Phase Lock Loop (PLL) techniques. DAFS techniques often provide excellent phase noise and switching speed performance but are often more complex, more costly, take up more volume, and consume more power than the other techniques. DDS technology’s primary attribute is frequency switching speed; however it is often encumbered by its lack of frequency coverage and spurious performance. DDS-based synthesizers have tremendous potential for future growth and application to SI as a result of rapid developments in GaAs, Si, and SiGe devices. The extension of the DDS usable bandwidth, together with spurious reduction, is the key improvement required for this technology to be an emerging trend in modular SI-based systems. Frequency synthesizers employing PLL technology are commonly used throughout the electronics industry and are extremely popular devices due to their simplicity, availability and relatively low costs.

Historically, T&M synthesizer developers have relied on Yttrium Iron Garnet (YIG) tuned oscillators featuring broadband operation and excellent phase noise performance. From a performance perspective, the main disadvantage of YIG technology is its slow switching speed; this drawback is the primary cause in the recent shift away from YIG-based designs to indirect techniques employing Voltage Controlled Oscillator (VCO) based technology [10]. This emerging synthesizer technology will be fueled by the capability to simultaneously provide fast frequency switching speed and reduction of the residual noise floor to extend the PLL bandwidths to much higher frequencies where solid state VCO noise becomes competitive with YIG devices. *Therefore, a near-term trend in SI is the emergence of fast switching/low phase noise indirect techniques employing VCO technology as a replacement for traditional YIG-based synthesizers [11] where signal quality and speed are of paramount importance—especially in military flight line and other forward level maintenance applications.*

### *D. Data Converters*

SI-based systems effect measurements (and generate signals) by employing numerical processing techniques which is inherently a digital process. However, the ATE interface to the UUT is typically analog and the ADC/DAC represents the interface between the analog and digital domains. Therefore, similar to frequency translation, the ADCs and DACs are essential (and critical) components to the SI architecture and advances in data converter technology have a major driving affect on SI performance because it is important to accurately reproduce the signals of interest prior to making a measurement or generating a stimulus signal. The challenge of SI data converters is to simultaneously maximize the accuracy and capture bandwidth, usually forcing the SI to employ multiple data converters because accuracy and bandwidth are inversely proportional [12]. However, empirical data show that we are seeing an increase in capture bandwidth (for a given accuracy) of approximately a factor of two every three years. *From an SI perspective, we predict that SI-based test systems will converge to single data converter architectures.*

From an ADC performance perspective, recent literature indicates that current and projected advances in sample rates are on track with market demands. However, advances in bandwidth performance for ADCs are projected to be less than required [13]. *The authors anticipate that future SI data converter requirements will focus on increased capture bandwidth, improved noise performance, and higher inter-modulation spurious performance in support of spectrum analysis related applications.*

New and emerging SI systems will be required to sample or synthesize higher frequencies—not only for higher IFs, but also for direct RF sampling and synthesis. In the future, direct RF sampling may well be the key to greatly simplified systems and lower SI costs with the caveat that their performance parameters must be comparable to, and cost competitive with, SI systems that employ classical RF/ $\mu$ W Up Converter/Down Converter frequency translation techniques. Should this event occur, it will be a defining moment in SI-based systems development. *The authors do not foresee the supplanting of classical RF/ $\mu$ W frequency translation techniques by digital*

technology in the foreseeable future. Much of the innovation over the last decade in high speed converter development has focused on improving the operation of converters at higher analog RF frequencies. However, while Input Bandwidth has improved significantly over the past 10 years, SFDR has not. A system with a large input bandwidth is less prone to slew rate limitations allowing the ADC to better track the signal input to the device. That is, for optimal spurious performance, a wide input bandwidth is desirable. However, by making the sample capacitance as small as possible, the resulting increase in input bandwidth allows more noise to enter the front end of the ADC and be spread over the Nyquist spectrum. This phenomenon has created an interesting tradeoff. In addition to improved spurious performance and a wider bandwidth, the circuitry allows more noise to pass to the sampling capacitor. This results in a lower ADC SNR due to increased input noise. *Along the ADC performance specification continuum, the authors anticipate that in the foreseeable future, input bandwidth and sample rates will continue to improve in an incremental manner. However, the other two primary data converter parameters of interest, SFDR and SNR, are not orthogonal and must always be traded off between one another. Also, since the SFDR BW product is constrained by the physical size of the sampling capacitor and the associated manufacturing processes employed in its implementation, the authors foresee that an improvement in SFDR performance will most likely require a new or enhanced technology to displace the standard CMOS processes currently in use [14].*

#### E. Multi-Bus Architectures

The T&M industry over the past five decades has made tremendous progress in the development of instrumentation data buses which facilitate the automation of the T&M process. Examples of mainstream buses are the General Purpose Interface (GPIB) bus, Universal Serial Bus (USB), VME Extensions for Instrumentation (VXI), PCI Extensions for Instrumentation (PXI), LAN Extension for Instrumentation (LXI), and the emerging hybrid parallel/serial bus architectures (PCI Express). Each of these buses satisfies a particular need in satisfying the primary user requirements such as system latency, bandwidth (speed and number of data I/O lanes), ease of installation and use, modularity, and data transmission range. The customer/user must choose the platform types that are right for a particular SI application or range applications. For example, the PXI bus and its PXI Express (PXIe) satisfy SI needs in terms of high speed data streaming up to 1 GB/sec from SI digitizers to a companion FPGA board for processing. Similarly, LXI and its associated LAN interface shines in remote control of SI applications, data transmission range, and widespread use. *The authors foresee that a future SI design trend will be the employment of multi-bus architectures in order to synthesize tailored SI end user solutions.*

An important aspect of the synthesis process with respect to legacy systems may be how to cost effectively re-engineer classical rack-and-stack systems into SI systems via employing a subset of available assets in order to create more flexible and better tailored ATS in concert with the end user's needs. The authors foresee the increased use of hybrid SI architectures in the out years as users employ "best of class" SI components,

regardless of form factor or bus I/O implementation, to implement their SI solutions. For example, a system could be configured employing GPIB, VXI, or LXI components to synthesize the SHE path due to the widespread availability of up converters/synthesizers and AWGs employing these instrumentation buses and/or formats. Similarly, a user could employ PXI controllers, down converters, FPGA boards, and ADCs in support of MHE functionality because of their size, speed, and low cost attributes. *Customization and flexibility in support of a customer's unique requirements will be the mantra of future SI solution architects and multi-bus systems will play a key role in this regard.*

### VIII. SUMMARY & CONCLUSIONS

Synthetic Instrumentation is an emerging technology that will transform the T&M industry in support of an increased customer focus on flexible, tailored, and cost-effective multi-purpose instrumentation. Transformation of the Synthetic Instrumentation paradigm from the early adopter phase to a global, mainstream solution will require acceptance and development of core SI supporting technologies, and support by a supply chain of leading T&M hardware and component manufacturers, as well as test software and facilitating software tool suppliers. This transformation will be necessary to satisfy customer need for faster, smaller, cost effective, and more information-intensive ATS which have long service lives and are compatible with the ubiquitous Personal Computer paradigm and its associated visual/parallel programming and data presentation tools.

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